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AB Kahng - Proceedings of the 2000 international symposium on Physical ..., 2000 - portal.acm.org
... objective and constraints) and the **floor- plan** quality that ... a connectivity- and timing-driven, near-legal **floorplan**. The result of global **floor**- planning can ...
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Handling soft modules in general nonslicing floorplan usingLagrangian relaxation - group of 5 »
FY Young, CCN Chu, WS Luk, YC Wong - Computer-Aided Design of Integrated Circuits and Systems, ..., 2001 - ieeexplore.ieee.org
... A nonslicing **floorplan** is one that is not restricted to be ... up horizontally or vertically to produce new **shape** curves for ... [11] use numerical **optimization** methods ...
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Fast hierarchical floorplanning with congestion and timing control - group of 3 »
A Ranjan, K Bazargan, M Sarrafzadeh - Computer Design, 2000. Proceedings. 2000 International ..., 2000 - ieeexplore.ieee.org
... our main focus has been the **optimization** of objectives ... the **shape** of the final **floorplan** is fixed ... Temperature Simulated Annealing on the **floor- plan** obtained by ...
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A floorplanning algorithm using rectangular Voronoi diagram andforce-directed block **shaping** - group of 2 »
SG Choi, CM Kyung - Computer-Aided Design, 1991. ICCAD-91. Digest of Technical ..., 1991 - ieeexplore.ieee.org
... Using Rectangular Voronoi Diagram and Force-Directed Block **Shaping** Sang-Gil ... formed by topological constraint reduction, and a legal **floor- plan** that satisfies ...
Cited by 6 - Web Search

Interconnect delay estimation models for synthesis and design planning - group of 10 »
J Cong, DZ Pan - Design Automation Conference, 1999. Proceedings of the ASP- ..., 1999 - ieeexplore.ieee.org
... with respect to a given **floor- plan**/placement, running ... model is used to guide the delay **optimization** and estimation ... DWS) [5] and continuous wire **shaping** (CWS) [6 ...
Cited by 47 - Web Search

Nonrectangular **shaping** and sizing of soft modules for floorplan-design improvement - group of 3 »
CCN Chu, EFY Young - Computer-Aided Design of Integrated Circuits and Systems, ..., 2004 - ieeexplore.ieee.org
... We used a subgradient **optimization** method to search ... OF SOFT MODULES FOR **FLOORPLAN**-DESIGN IMPROVEMENT 79 ... HH Yang, "On extending slicing **floor- plans** to handle ...
Cited by 2 - Web Search - BL Direct

Macro Block Based FPGA Floorplanning - group of 5 »
J Shi, A Randhar, D Bhatia - doi.ieeecomputersociety.org
... The best **floorplan** with timing **optimization** is selected, and ... produce a more compact legal FPGA **floor- plan** result. ... in order to optimize the legal **floorplan** area ...
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... com- putation, the tree enumeration and cost **optimization** processes should ... be an exponential number of distinct **floor- plan** trees for an n-cell **floorplan**. ...
Cited by 8 - Web Search - BL Direct

Buffer block planning for interconnect-driven floorplanning - group of 19 »
J Cong, T Kong, DZ Pan - Proc. ICCAD, 1999 - doi.ieeecomputersociety.org
... us a lot of flexibility to **plan** a buffer ... used as a key element for interconnect-driven **floor**- planning ... planning (BBP) problem: given an initial **floorplan** and the ...
Cited by 98 - Web Search - BL Direct

Floorplan **optimization** on multiprocessors
S Arvindam, V Kumar, VN Rao - Computer Design: VLSI in Computers and Processors, 1989. ..., 1989 - ieeexplore.ieee.org
... only work for a special kind of **floor plans** called slicing ... from Section 3 that due to **optimization** #3, it ... a parallel B&B program for **floorplan** op- timization ...
Cited by 11 - Web Search

A robust framework for hierarchical floorplanning with integratedglobal wiring
T Lengauer, R Muller - Computer-Aided Design, 1990. ICCAD-90. Digest of Technical ..., 1990 - ieeexplore.ieee.org
... In early systems, wiring followed the computation of the **floor- plan**. ... We allow for the most general **optimization** during **floorplan sizing** that is still ...
Cited by 18 - Web Search

Floorplan **Sizing** by Linear Programming Approximation - group of 9 »
P Chen, ES Kuh - DAC 2000 - doi.ieeecomputersociety.org
... However, the **size** of the problem it can handle is ... the analogy between the resistive network and a **floorplan**. ... they use is an unconstrained **optimization** with a ...
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Rectangle-packing-based module placement - group of 9 »
H Murata, K Fujiyoshi, S Nakatake, Y Kajitani - Proceedings of the 1995 IEEE/ACM international conference on ..., 1995 - portal.acm.org
... angular modules of arbitrary **size**, place them with- ... for successful **optimization** is in the introduction of a P-admissible solution space, which is a nite set of ...
Cited by 181 - Web Search - BL Direct

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J Cong, DZ Pan - Design Automation Conference, 1999. Proceedings of the ASP- ..., 1999 - ieeexplore.ieee.org
... interconnects with respect to a given **floor- plan**/placement, running ... To make use of those **optimization** programs, a ... number of wire widths and buffer **sizes**, etc. ...
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Power supply noise analysis methodology for deep-submicron VLSI chip design - group of 9 »
HH Chen, DD Ling - Proceedings of the 34th annual conference on Design ... - doi.ieeecomputersociety.org